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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO
10/710,662	07/27/2004	Jui-Tsen Huang	12336-US-PA	4661
31561 75	90 11/27/2006		EXAMINER	
JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE 7 FLOOR-1, NO. 100 ROOSEVELT ROAD, SECTION 2			HARRISON, MONICA D	
			ART UNIT	PAPER NUMBER
TAIPEI, 100			2813	
TAIWAN			DATE MAILED: 11/27/2006	

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)			
	10/710,662	HUANG, JUI-TSEN			
Office Action Summary	Examiner	Art Unit			
	Monica D. Harrison	2813			
The MAILING DATE of this communication app					
Period for Reply					
A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING DATE - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication.  If NO period for reply is specified above, the maximum statutory period was period to reply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be tim vill apply and will expire SIX (6) MONTHS from cause the application to become ABANDONEI	l. ely filed the mailing date of this communication. D (35 U.S.C. § 133).			
Status					
1) ☐ Responsive to communication(s) filed on <u>06 Jules</u> 2a) ☐ This action is FINAL. 2b) ☐ This      3) ☐ Since this application is in condition for allower closed in accordance with the practice under E	action is non-final. nce except for formal matters, pro				
Disposition of Claims					
4) ☐ Claim(s) 1-20 is/are pending in the application. 4a) Of the above claim(s) is/are withdraw 5) ☐ Claim(s) is/are allowed. 6) ☐ Claim(s) 1-20 is/are rejected. 7) ☐ Claim(s) is/are objected to. 8) ☐ Claim(s) are subject to restriction and/or	vn from consideration.				
Application Papers					
9) The specification is objected to by the Examine 10) The drawing(s) filed on is/are: a) accomplicated any not request that any objection to the Replacement drawing sheet(s) including the correct 11) The oath or declaration is objected to by the Example 11.	epted or b) objected to by the liderawing(s) be held in abeyance. See ion is required if the drawing(s) is obj	e 37 CFR 1.85(a). ected to. See 37 CFR 1.121(d).			
Priority under 35 U.S.C. § 119					
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  a) All b) Some * c) None of:  1. Certified copies of the priority documents have been received.  2. Certified copies of the priority documents have been received in Application No  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  * See the attached detailed Office action for a list of the certified copies not received.					
Attachment(s)  1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date	4)  Interview Summary Paper No(s)/Mail Da 5)  Notice of Informal F 6)  Other:	nte			

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#### **DETAILED ACTION**

1. Applicant's remarks field 7/6/06 have been entered.

## Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Yu et al (6,571,485 B1).

- 2. Regarding claim 1, Yu et al discloses a stress relieving method for a wafer, comprising the steps of: providing a wafer (Figure 2, reference 200) with a dielectric layer thereon (Figure 2, reference 205), wherein the wafer is divided into a first area and a second area such that at least no circuits are formed on the dielectric layer within the first area (Figure 2); forming a plurality of first openings in the dielectric layer within the first area (Figure 2, reference 207); and forming a first material layer over the wafer (Figure 2, reference 208), wherein the upper surface of the first material layer has pits at locations over the first openings (Figure 2, reference 211).
- Regarding claim 2, Yu et al discloses wherein the first area comprises a scribe line (column 1, lines 30-35)
- 4. Regarding claim 3, Yu et al discloses wherein the second area comprises a region for forming a die (Figure 2, reference 202).

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5. Regarding claim 4, Yu et al discloses wherein the first area comprises a scribe line (column 1, lines 30-35).

- 6. Regarding claim 5, Yu et al discloses wherein the first area and the second area are both regions for forming a die (Figure 2).
- 7. Regarding claim 6, Yu et al discloses wherein forming a plurality of second openings in the first dielectric layer within the second area (Figure 2, reference 206) at the same time and than depositing material into the second openings (Figure 2, reference 204) to form a plurality of second material layers.
- 8. Regarding claim 7, Yu et al discloses wherein the first opening is not deep enough to expose a film layer underneath the dielectric layer (Figure 2, reference 207).
- 9. Regarding claim 8, Yu et al discloses wherein the first opening exposes a film layer underneath the dielectric layer (Figure 2, reference 206).
- 10. Regarding claim 9, Yu et al discloses wherein the first material layer is fabricated from a dielectric material or a metal material (Figure 2, reference 204; metal)
- Regarding claim 10, Yu et al discloses a stress relieving method for a wafer, comprising the steps of: providing a wafer (Figure 2, reference 200) with a dielectric layer thereon (Figure 2, reference 205), wherein the wafer is divided into a first area and a second area such that no circuits arc formed within the first area (Figure 2); forming a first material layer over the wafer (Figure 2, reference 204); and removing a portion of the first material layer within the first area to form a plurality of first openings (column 1, lines 44-47).
- 12. Regarding claim 11, Yu et al discloses wherein the first area comprises a scribe line (column 1, lines 30-35).

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13. Regarding claim 12, Yu et al discloses wherein the second area comprises a region for forming a die (Figure 2, reference 202).

- 14. Regarding claim 13, Yu et al discloses wherein the first area comprises a scribe line (column 1, lines 30-35).
- 15. Regarding claim 14, Yu et al discloses wherein the first area and the second area are both regions for forming a die (Figure 2).
- 16. Regarding claim 15, Yu et al discloses wherein the first opening is not deep enough to expose the dielectric layer (Figure 2, reference 207).
- 17. Regarding claim 16, Yu et al discloses wherein the first opening exposes the dielectric layer (Figure 2, reference 206).
- 18. Regarding claim 17, Yu et al discloses wherein forming a plurality of second openings in the dielectric layer within the second area (Figure 2, reference 206); and depositing material into the second openings to form a plurality of second material layers (Figure 2, reference 208).
- 19. Regarding claim 18, Yu et al discloses wherein first material layer is fabricated from a dielectric material or a metal material (Figure 2, reference 204).

### Claim Rejections - 35 USC § 103

Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu et al (6,571,485 B1) in view of Fahey et al (5,447,884).

20. Yu et al discloses all above claimed subject matter except wherein the first material layer is a high stress dielectric layer (claims 19 and 20).

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Fahey et al discloses wherein the first material layer is a high stress dielectric layer (Figure 5, reference 60).

It is obvious, at the time the invention was made, for one having ordinary skill in the art, to modify Yu et al, with the teachings of Fahey et al, for the purpose of forming a shallow trench isolation in integrated circuits.

## Response to Arguments

Applicant's arguments, see pp.1-9, filed 7/6/06, with respect to the rejection(s) of claim(s) 1-20 under 35 USC 102 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Yu et al (6,571,485 B1) and Fahey et al (5,447,884).

#### Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica D. Harrison whose telephone number is 571-272-1959. The examiner can normally be reached on M-F 7:00am-3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <a href="http://pair-direct.uspto.gov">http://pair-direct.uspto.gov</a>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Monica D. Harrison AU 2813

mdh

November 21, 2006

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